IN THE CLAIMS

1. (Original) A device comprising:

a memory array;

a first data path connected to the memory array for transferring data at a first speed; and

a second data path connected to the memory array for transferring data at a second speed.

2. (Original) The device of claim 1, wherein each of the first and second data paths is a bi-directional data path.

3. (Currently Amended) A device comprising:

a memory array;

a first data path connected to the memory array for transferring data at a first speed;

a second data path connected to the memory array for transferring data at a second speed; and ~~The device of claim 1 further comprising~~

a strobe transceiver circuit connected to the first data path for transferring data to and from the first data path at the first speed, and connected to the second data path for transferring data to and from the second path at the second speed.

4. (Original) The device of claim 3 further comprising a data transceiver circuit connected to the second data path for transferring data to and from the second path at the second speed.

5. (Original) The device of claim 4, wherein each of the strobe and data transceiver circuits includes a plurality of transceivers, each of the transceivers in the strobe transceiver circuit having elements matching elements of each of the transceivers in the data transceiver circuit.

6. (Original) A device comprising:

a memory array;

a first data path connected to the memory array for transferring data at a first speed;

a second data path connected to the memory array for transferring data at a second speed;

a plurality of strobe transceivers connected to the first and second data paths for transferring data to and from the first data path at the first speed and for transferring data to and from the second data path at the second speed; and

a plurality of data transceivers connected to the second data path for transferring data to and from the second path at the second speed.

7. (Original) The device of claim 6, wherein:

the first data path is configured to transfer data to and from the memory array at the first speed in one mode; and

the second data path is configured to transfer data to and from the memory array at the second speed in another mode.

8. (Original) The device of claim 6, wherein the first data path is configured to transfer data at the first speed in a test mode, and the second data path is configured to transfer data at the second speed in the test mode and in a normal mode.

9. (Original) The device of claim 6, wherein the plurality of strobe transceivers includes:

a number of write strobe transceivers for receiving data from the first data path at the first speed and for providing write strobe signals to the second data path at the second speed; and

a number of read strobe transceivers for providing data to the first data path at the first speed and for receiving read strobe signals from the second data path at the second speed.

10. (Original) The device of claim 6, wherein each of the strobe transceivers and each of the data transceivers have matching elements.

11. (Original) The device of claim 6, wherein each of the strobe transceivers and each of the data transceivers have equal number of elements.

12. (Currently Amended) A device comprising:

a memory array;

a first data path connected to the memory for transferring data at a first speed;

a second data path connected to the memory array for transferring data at a second speed;

a plurality data transceivers connected to the second data paths for transferring data to and from the memory array via the second data paths;

a plurality write strobe transceivers connected to the first and second data paths for receiving data from the first data path in a test mode, and for providing write strobe signals to the second data path in one of the test mode and a normal mode; and

a plurality read strobe transceivers connected to the first and second data paths for ~~proving~~ providing data to the first data path in the test mode, and for receiving read strobe signals from the second data path in one of the test mode and the normal mode.

13. (Currently Amended) The device of claim 12, wherein each of the write strobe transceivers is configured to receive data from the first data path at the first speed in a read operation in [[a]] the test mode.

14. (Original) The device of claim 13, wherein each of the write strobe transceivers is further configured to provide one of the write strobe signals to the second data path at the second speed in a write operation in the test mode.

15. (Original) The device of claim 13, wherein each of the write strobe transceivers is further configured to provide one of the write strobe signals to the second data path at the second speed in a write operation in a normal mode.

16. (Original) The device of claim 12, wherein each of the read strobe transceivers is configured to provide data to the first data path at the first speed in a write operation in a test mode.

17. (Original) The device of claim 16, wherein each of the read strobe transceivers is further configured to receive one of the read strobe signals from the second data path at the second speed in a read operation in a test mode.

18. (Original) The device of claim 16, wherein each of the read strobe transceivers is further configured to receive one of the read strobe signals from the second data path at the second speed in a read operation in a normal mode.

19. (Original) The device of claim 12, wherein each of the data transceivers is configured to provide data to the second data path at the second speed in a write operation of one in a test mode and a normal mode and configured to receive data from the second data path at the second speed in a read operation of one of the test mode and the normal mode.

20. (Original) The device of claim 12, wherein each of the write strobe transceivers, each of the read strobe transceivers, and each of the data transceivers have equal number of matching elements.

21. (Original) The device of claim 12, wherein each of the write strobe transceivers includes:
an input circuit connected to the second data path; and
an output circuit connected to the first data path.

22. (Original) The device of claim 21, wherein each of the read strobe transceivers includes:
an input circuit connected to the first data path; and
an output circuit connected to the second data path.

23. (Original) The device of claim 22, wherein each of the data transceivers includes:
an input circuit connected to the second data path; and
an output circuit connected to the second data path.

24. (Original) The device of claim 23, wherein the input circuits of the write strobe transceivers, read strobe transceivers, and data transceivers are identical.

25. (Original) The device of claim 24, wherein the output circuits of the write strobe transceivers, read strobe transceivers, and data transceivers are identical.

26. (Original) A device comprising:

a memory array;

a first bi-directional data path connected to the memory array;

a second bi-directional data path connected to the memory array;

a plurality of strobe transceivers connected to the first and second bi-directional data paths;

a plurality of data transceivers connected to the second bi-directional data path; and

a path selector connected between the memory array and the first and second bi-directional data paths for selecting one of the first and second bi-directional data paths for transferring data between the memory array and one of the first and second bi-directional data paths.

27. (Original) The device of claim 26, wherein the first bi-directional data path is configured to transfer data at a first speed.

28. (Original) The device of claim 27, wherein the second bi-directional data path is configured to transfer data at a second speed.

29. (Currently Amended) The device of claim 26, wherein the strobe transceivers are configured to ~~transferring~~ transfer data to and from the first bi-directional data path at the first speed and ~~for transferring~~ to transfer data to and from the second bi-directional data path at the second speed.

30. (Original) The device of claim 29, wherein the data transceivers are configured to transfer data to and from the second bi-directional data path at the second speed.

31. (Original) The device of claim 30, wherein each of the strobe transceivers and each of the data transceivers have matching elements.

32. (Original) The device of claim 26, wherein the first bi-directional data path includes:

a data input/output circuit connected to the path selector;

an internal circuit; and

a select unit connected to the input/output circuit and the internal circuit for selecting a route to transfer data between the strobe transceivers and one of the input/output circuit and the internal circuit.

33. (Original) The device of claim 32, wherein the input/output circuit includes:

a plurality of input latches connected to the select unit for receiving data from the strobe transceivers based on a first combination of select signals; and

a plurality of output latches connected to the select unit for outputting data to the strobe transceivers based on a second combination of the select signals.

34. (Original) The device of claim 33, wherein the input/output circuit further includes a compression and decompression engine connected to the input and output latches for compressing data transferred from the input latches and for decompressing data transferred to the output latches.

35. (Original) The device of claim 32, wherein the internal circuit includes:

a control path connected to the select unit for receiving control data from the strobe transceivers based on a first combination of the select signals; and

a feedback path connected to the select unit for providing feedback data to the strobe transceivers based on a second combination of the select signals.

36. (Original) A device comprising:

a first data path and a second data path;

a first group of transceivers, each having an input circuit connected to the second data path and an output circuit connected to the first data path;

a second group of transceivers, each having an input circuit connected to the first data path and an output circuit connected to the second data path; and

a third group of transceivers, each having an input circuit connected to the second data path and an output circuit connected to the second data path.

37. (Original) The device of claim 36, wherein each transceiver of the first group of transceivers, each transceiver of the second group of transceivers, and each transceiver of the third group of transceivers have equal number of elements.

38. (Original) The device of claim 37, wherein each of the first and second data paths is a bi-directional data path.

39. (Original) The device of claim 36, wherein the input circuits of transceivers of the first, second, and third groups of transceivers are identical.

40. (Original) The device of 39, wherein the output circuits of transceivers of the first, second, and third groups of transceivers are identical.

41. (Original) The device of 36 further comprising a memory array connected to the first and second data path.

42. (Original) The device of claim 41, wherein the device further comprising a path selector connected in a path between the memory array and the first and second data paths.

43. (Original) The device of claim 42, wherein each of the first and second group of transceivers is configured to transferred data to and from the first data path at a first speed and configured to transferred data to and from the second data path at a second speed.

44. (Original) The device of claim 43, wherein the third group of transceivers is configured to transfer data to and from the second data path at the first speed.

45. (Original) A system comprising:

a processor; and

a memory device connected to the processor, the memory device including:

a memory array;

a first data path connected to the memory array and configured for transferring data at a first speed;

a second data path connected to the memory array and configured for transferring data at a second speed; and

a plurality of transceivers connected to the first and second data paths.

46. (Original) The system of claim 45, wherein each of the first and the second data paths is a bi-directional data path.

47. (Original) The system of claim 45, wherein the plurality of transceivers includes a plurality of strobe transceivers connected to the first data path for transferring data at the first speed, and connected to the second data path for transferring data at the second speed.

48. (Original) The system of claim 47, wherein the plurality of transceivers further includes a plurality of data transceivers connected to the second data path for transferring data at the second speed.

49. (Original) The system of claim 48, wherein the each of the plurality of strobe transceivers and each of the plurality data transceivers includes equal number of elements.

50. (Original) The system of claim 48, wherein the each of the plurality of strobe transceivers and each of the plurality of data transceivers includes matching elements.

51.-85. (Canceled)